12-BIT 8-CHANNEL SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH I²C™ INTERFACE

Check for Samples: ADS7828-Q1

FEATURES

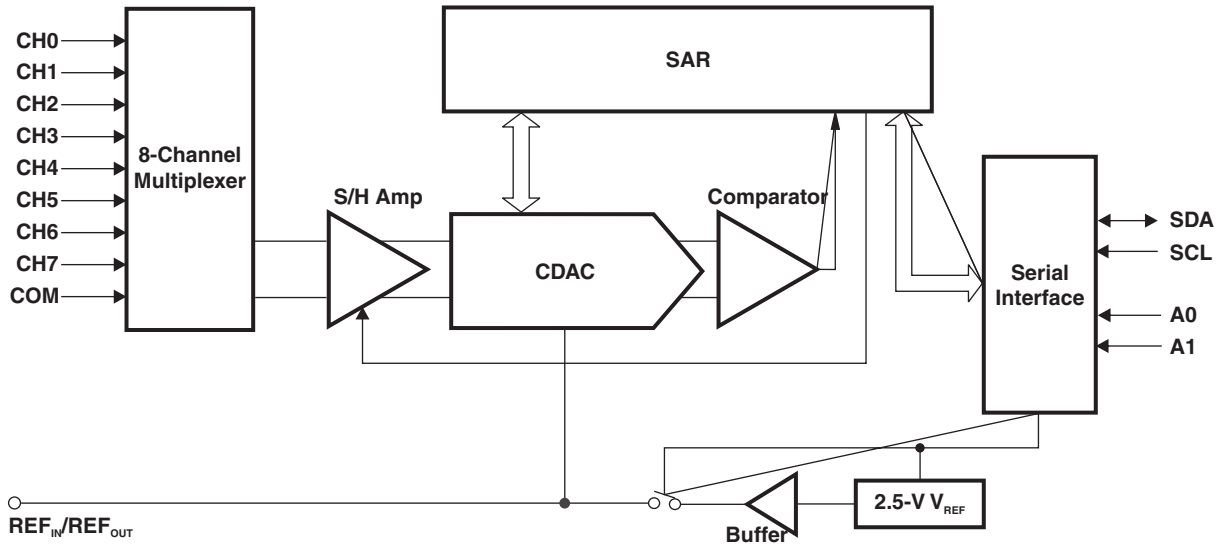
- **Qualified for Automotive Applications**
- **8-Channel Multiplexer**
- **50-kHz Sampling Rate**
- **No Missing Codes**
- **2.7-V to 5-V Operation**
- **Internal 2.5-V Reference**
- **I²C™ Interface Supports Standard, Fast, and High-Speed Modes**
- **TSSOP-16 Package**

APPLICATIONS

- **Voltage-Supply Monitoring**
- **Isolated Data Acquisition**
- **Transducer Interfaces**
- **Battery-Operated Systems**
- **Remote Data Acquisition**

DESCRIPTION

The ADS7828 is a single-supply low-power 12-bit data acquisition device that features a serial I²C interface and an 8-channel multiplexer. The analog-to-digital (A/D) converter features a sample-and-hold amplifier and internal asynchronous clock. The combination of an I²C serial 2-wire interface and micropower consumption makes the ADS7828 ideal for applications requiring the A/D converter to be close to the input source in remote locations and for applications requiring isolation. The ADS7828 is available in a TSSOP-16 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

I2C is a trademark of NXP Semiconductors.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

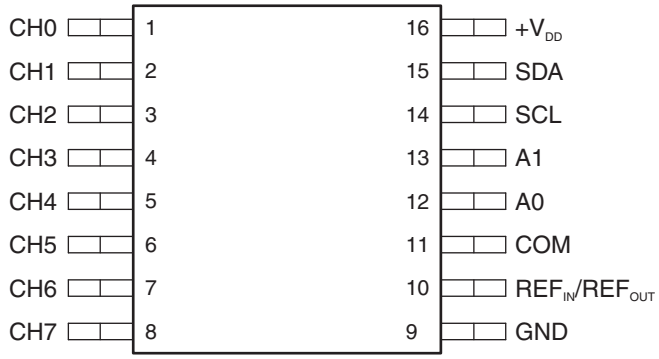
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	PACKAGE (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	±2	TSSOP – PW	Reel of 2500	ADS7828EIPWRQ1	7828EI
	±1			ADS7828EBIPWRQ1	PREVIEW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PW PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
CH0	1	Analog input channel 0
CH1	2	Analog input channel 1
CH2	3	Analog input channel 2
CH3	4	Analog input channel 3
CH4	5	Analog input channel 4
CH5	6	Analog input channel 5
CH6	7	Analog input channel 6
CH7	8	Analog input channel 7
GND	9	Analog ground
REF_{IN}/REF_{OUT}	10	Internal 2.5-V reference / external reference input
COM	11	Common to analog input channel
A0	12	Slave address bit 0
A1	13	Slave address bit 1
SCL	14	Serial clock
SDA	15	Serial data
$+V_{DD}$	16	Power supply, 3.3 V (nominal)

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage		–0.3 V to 6 V
V_{IN}	Digital input voltage		–0.3 V to ($+V_{DD}$ + 0.3 V)
θ_{JA}	Thermal impedance, junction to free air(3) (4)		108.4°C/W
T_A	Operating free-air temperature		–40°C to 85°C
T_J	Operating virtual-junction temperature		150°C
T_{stg}	Storage temperature		–65°C to 150°C
T_{lead}	Lead temperature during soldering	Vapor phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND terminal.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

		TEST CONDITIONS	RATING
ESD	Electrostatic discharge rating	Human-Body Model (HBM)	2000 V
		Machine Model (MM)	200 V
		Charged-Device Model (CDM)	1000 V

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$+V_{DD}$	Supply voltage	2.7-V nominal	2.7		3.6	V
		5-V nominal	4.75	5	5.25	
V_{IN}	Analog input voltage	Positive input	–0.2		$+V_{DD}$ + 0.2	V
		Negative input	–0.2		0.2	
		Full-scale differential (Positive input – Negative input)	0		V_{REF}	V
$V_{IN(REF)}$	Voltage reference input voltage		0.05		$+V_{DD}$	V
V_{IH}	High-level digital input voltage		0.7 × $+V_{DD}$		$+V_{DD}$ + 0.5	V
V_{IL}	Low-level digital input voltage		–0.3		0.3 × $+V_{DD}$	V
T_A	Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

$+V_{DD}$ = 2.7 V, V_{REF} = 2.5 V, SCL clock frequency = 3.4 MHz (high-speed mode), over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS7828E			ADS7828EB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Analog Input									
I_{leak}	Leakage current			±1			±1		µA
C_i	Input capacitance			25			25		pF
Overall Performance									
	No missing codes		12			12			bits
	Integral linearity error			±1	±2		±0.5	±1	LSB(1)
	Differential linearity error			±1			±0.5	–1/+2	LSB
	Offset error			±1	±3		±0.75	±2	LSB
	Offset error match			±0.2	±1		±0.2	±1	LSB
	Gain error			±1	±4		±0.75	±3	LSB
	Gain error match			±0.2	±1		±0.2	±1	LSB
V_n	Noise	RMS		33			33		µV
PSRR	Power-supply ripple rejection			82			82		dB
Sampling Dynamics									
	Throughput frequency	High-speed mode: SCL = 3.4 MHz			50			50	kHz
		Fast mode: SCL = 400 kHz			8			8	
		Standard mode: SCL = 100 kHz			2			2	
	Conversion time			6			6		µs
AC Accuracy									
THD	Total harmonic distortion(2)	V_{IN} = 2.5 V_{PP} at 10 kHz		–82			–82		dB
	Signal-to- ratio	V_{IN} = 2.5 V_{PP} at 10 kHz		72			72		dB
	Signal-to-(noise+distortion) ratio	V_{IN} = 2.5 V_{PP} at 10 kHz		71			71		dB
	Spurious-free dynamic range	V_{IN} = 2.5 V_{PP} at 10 kHz		86			86		dB
	Channel-to-channel isolation			120			120		dB
Voltage Reference Output									
V_O	Output voltage		2.475	2.5	2.525	2.475	2.5	2.525	V
	Internal reference drift			15			15		ppm/°C
z_o	Output impedance	Internal reference on		110			110		Ω
		Internal reference off		1			1		GΩ
I_Q	Quiescent current			850			850		µA
Voltage Reference Input									
r_i	Input resistance			1			1		GΩ
	Current drain			20			20		µA
Digital Input/Output									
V_{OL}	Low-level output voltage	Minimum 3-mA sink current			0.4			0.4	V
I_{IH}	High-level input current	V_{IH} = $+V_{DD}$ + 0.5 V			10			10	µA
I_{IL}	Low-level input current	V_{IL} = –0.3 V	–10			–10			µA

(1) LSB means least significant bit; with V_{REF} equal to 2.5 V, one LSB is 610 µV.
(2) THD is measured to the ninth harmonic.

ELECTRICAL CHARACTERISTICS (continued)

$+V_{DD}$ = 2.7 V, V_{REF} = 2.5 V, SCL clock frequency = 3.4 MHz (high-speed mode), over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS7828E			ADS7828EB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply									
I_Q	Quiescent current	High-speed mode: SCL = 3.4 MHz		225	320		225	320	μA
		Fast mode: SCL = 400 kHz		100			100		
		Standard mode: SCL = 100 kHz		60			60		
P_D	Power dissipation	High-speed mode: SCL = 3.4 MHz		675	1000		675	1000	μW
		Fast mode: SCL = 400 kHz		300			300		
		Standard mode: SCL = 100 kHz		180			180		
	Power-down current with wrong address selected	High-speed mode: SCL = 3.4 MHz		70			70		μA
		Fast mode: SCL = 400 kHz		25			25		
		Standard mode: SCL = 100 kHz		6			6		
I_{PD}	Full power-down current	SCL pulled high, SDA pulled high		400	3000		400	3000	nA

ELECTRICAL CHARACTERISTICS

$+V_{DD}$ = 5 V, V_{REF} = External 5 V, SCL clock frequency = 3.4 MHz (high-speed mode), over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS7828E			ADS7828EB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Analog Input									
I_{leak}	Leakage current			±1			±1		µA
C_i	Input capacitance			25			25		pF
Overall Performance									
	No missing codes		12			12			bits
	Integral linearity error			±1	±2		±0.5	±1	LSB(1)
	Differential linearity error			±1			±0.5	–1/+2	LSB
	Offset error			±1	±3		±0.75	±2	LSB
	Offset error match				±1.5			±1	LSB
	Gain error			±1	±3		±0.75	±2	LSB
	Gain error match				±1			±1	LSB
V_n	Noise	RMS		33			33		µV
PSRR	Power-supply ripple rejection			82			82		dB
Sampling Dynamics									
	Throughput frequency	High-speed mode: SCL = 3.4 MHz			50			50	kHz
		Fast mode: SCL = 400 kHz			8			8	
		Standard mode: SCL = 100 kHz			2			2	
	Conversion time			6			6		µs
AC Accuracy									
THD	Total harmonic distortion(2)	V_{IN} = 2.5 V_{PP} at 10 kHz		–82			–82		dB
	Signal-to- ratio	V_{IN} = 2.5 V_{PP} at 10 kHz		72			72		dB
	Signal-to-(noise+distortion) ratio	V_{IN} = 2.5 V_{PP} at 10 kHz		71			71		dB
	Spurious-free dynamic range	V_{IN} = 2.5 V_{PP} at 10 kHz		86			86		dB
	Channel-to-channel isolation			120			120		dB
Voltage Reference Output									
V_O	Output voltage		2.475	2.5	2.525	2.475	2.5	2.525	V
	Internal reference drift			15			15		ppm/°C
z_o	Output impedance	Internal reference on		110			110		Ω
		Internal reference off		1			1		GΩ
I_Q	Quiescent current			1300			1300		µA
Voltage Reference Input									
r_i	Input resistance			1			1		GΩ
	Current drain			20			20		µA
Digital Input/Output									
V_{OL}	Low-level output voltage	Minimum 3-mA sink current			0.4			0.4	V
I_{IH}	High-level input current	V_{IH} = $+V_{DD}$ + 0.5 V			10			10	µA
I_{IL}	Low-level input current	V_{IL} = –0.3 V	–10			–10			µA

(1) LSB means least significant bit; with V_{REF} equal to 5 V, one LSB is 1.22 mV.
(2) THD is measured to the ninth harmonic.

ELECTRICAL CHARACTERISTICS (continued)

$+V_{DD}$ = 5 V, V_{REF} = External 5 V, SCL clock frequency = 3.4 MHz (high-speed mode), over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS7828E			ADS7828EB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply									
I_Q	Quiescent current	High-speed mode: SCL = 3.4 MHz		750	1000		750	1000	µA
		Fast mode: SCL = 400 kHz		300			300		
		Standard mode: SCL = 100 kHz		150			150		
P_D	Power dissipation	High-speed mode: SCL = 3.4 MHz		3.75	5		3.75	5	µW
		Fast mode: SCL = 400 kHz		1.5			1.5		
		Standard mode: SCL = 100 kHz		0.75			0.75		
	Power-down current with wrong address selected	High-speed mode: SCL = 3.4 MHz		400			400		µA
		Fast mode: SCL = 400 kHz		150			150		
		Standard mode: SCL = 100 kHz		35			35		
I_{PD}	Full power-down current	SCL pulled high, SDA pulled high		400	3000		400	3000	nA

SWITCHING CHARACTERISTICS(1) (2)

$+V_{DD}$ = 2.7 V, over operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	
		High-speed mode	C_b = 100 pF max		3.4	MHz
			C_b = 400 pF max		1.7	
t_{BUF}	Bus free time between Stop and Start conditions	Standard mode		4.7		µs
		Fast mode		1.3		
$t_{HD;\ STA}$	Hold time (repeated) Start condition	Standard mode		4		µs
		Fast mode		600		ns
		High-speed mode		160		
t_{low}	Low period of the SCL clock	Standard mode		4.7		µs
		Fast mode		1.3		
		High-speed mode(3)	C_b = 100 pF max	160		ns
			C_b = 400 pF max	320		
t_{high}	High period of the SCL clock	Standard mode		4		µs
		Fast mode		600		ns
		High-speed mode(3)	C_b = 100 pF max	60		
			C_b = 400 pF max	120		
$t_{SU;\ STA}$	Setup time for a repeated Start condition	Standard mode		4.7		µs
		Fast mode		600		ns
		High-speed mode		160		
$t_{SU;\ DAT}$	Data setup time	Standard mode		250		ns
		Fast mode		100		
		High-speed mode		10		
$t_{HD;\ DAT}$	Data hold time	Standard mode		0	3.45	µs
		Fast mode		0	0.9	
		High-speed mode(3) (4)	C_b = 100 pF max	0	82	ns
			C_b = 400 pF max	0	162	
t_{rCL}	Rise time of SCL signal	Standard mode			1000	ns
		Fast mode		20 + 0.1C_b	300	
		High-speed mode(3)	C_b = 100 pF max	10	40	
			C_b = 400 pF max	20	80	
t_{rCL1}	Rise time of SCL signal after a repeated Start condition and after an acknowledge bit	Standard mode			1000	ns
		Fast mode		20 + 0.1C_b	300	
		High-speed mode(3)	C_b = 100 pF max	10	80	
			C_b = 400 pF max	20	160	
t_{fCL}	Fall time of SCL signal	Standard mode			300	ns
		Fast mode		20 + 0.1C_b	300	
		High-speed mode(3)	C_b = 100 pF max	10	40	
			C_b = 400 pF max	20	80	
t_{rDA}	Rise time of SDA signal	Standard mode			1000	ns
		Fast mode		20 + 0.1C_b	300	
		High-speed mode(3)	C_b = 100 pF max	10	80	
			C_b = 400 pF max	20	160	

(1) All values referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.
(2) Not production tested, except for the parameter $t_{HD;\ DAT}$, data hold time, high-speed mode, C_b = 100 pF max.
(3) For bus line loads (C_B) between 100 pF and 400 pF, the timing parameters must be linearly interpolated.
(4) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

SWITCHING CHARACTERISTICS (1) (2) (continued)

$+V_{DD}$ = 2.7 V, over operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{fDA}	Fall time of SDA signal	Standard mode			300	ns
		Fast mode		20 + 0.1C_b	300	
		High-speed mode (3)	C_b = 100 pF max	10	80	
			C_b = 400 pF max	20	160	
$t_{SU;\ STO}$	Setup time for Stop condition	Standard mode		4		µs
		Fast mode		600		ns
		High-speed mode		160		
C_b	Capacitive load for SDA or SCL				400	pF
t_{SP}	Pulse width of spike suppressed	Fast mode			50	ns
		High-speed mode			10	
V_{nH}	Noise margin at the high level for each connected device (including hysteresis)			0.2 × V_{DD}		V
V_{nL}	Noise margin at the low level for each connected device (including hysteresis)			0.1 × V_{DD}		V

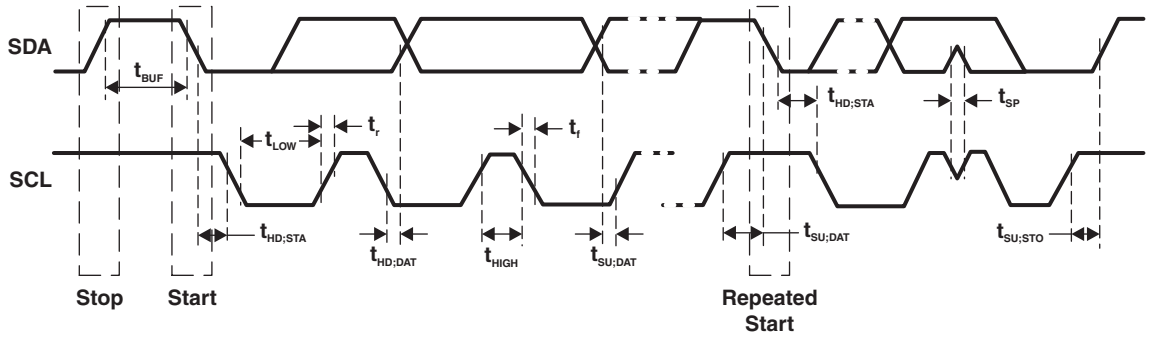
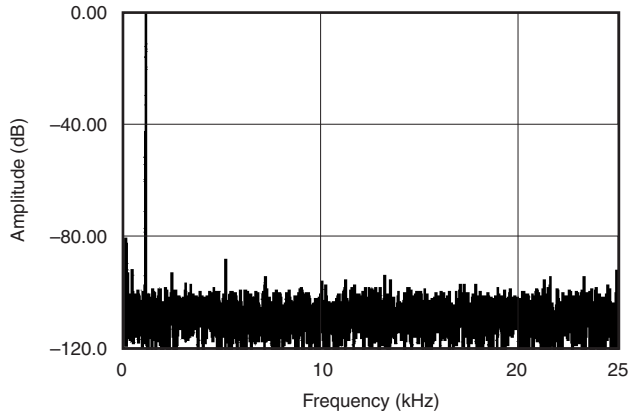


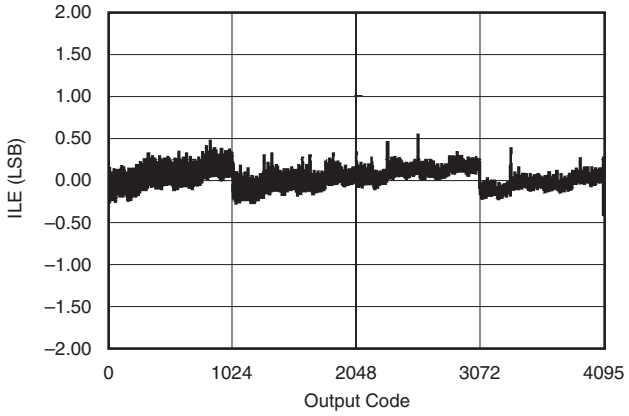
Figure 1. I^2C Timing

TYPICAL CHARACTERISTICS

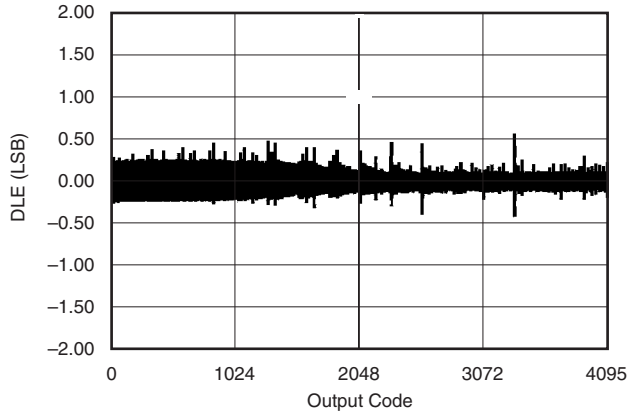
FREQUENCY SPECTRUM
(4096 Point FFT: f_{IN} = 1 kHz, 0 dB)



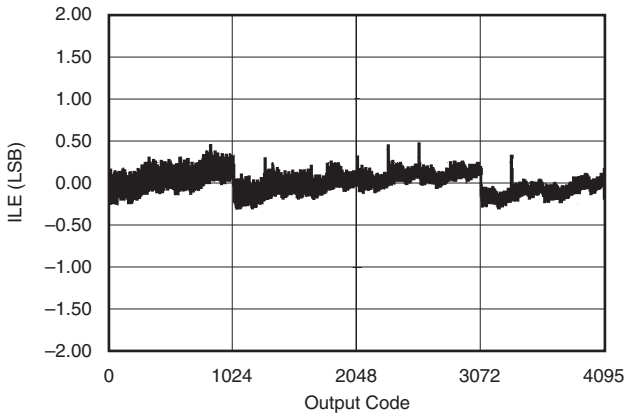
INTEGRAL LINEARITY ERROR vs CODE
(2.5V Internal Reference)



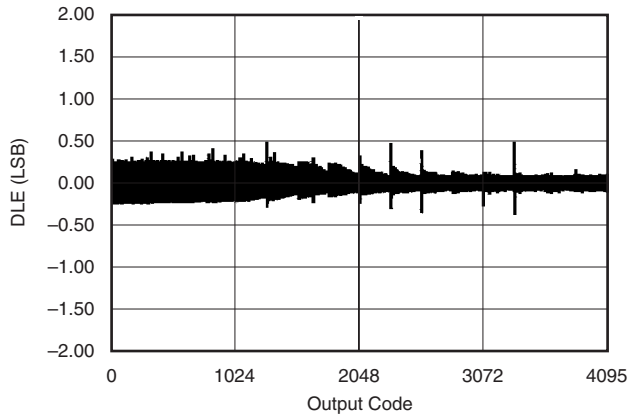
DIFFERENTIAL LINEARITY ERROR vs CODE
(2.5-V Internal Reference)



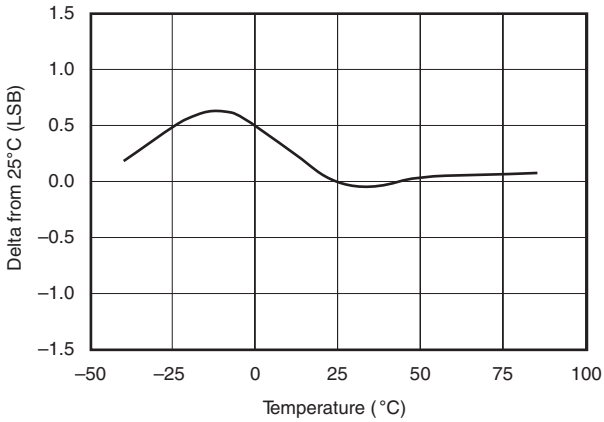
INTEGRAL LINEARITY ERROR vs CODE
(2.5-V External Reference)



DIFFERENTIAL LINEARITY ERROR vs CODE
(2.5-V External Reference)

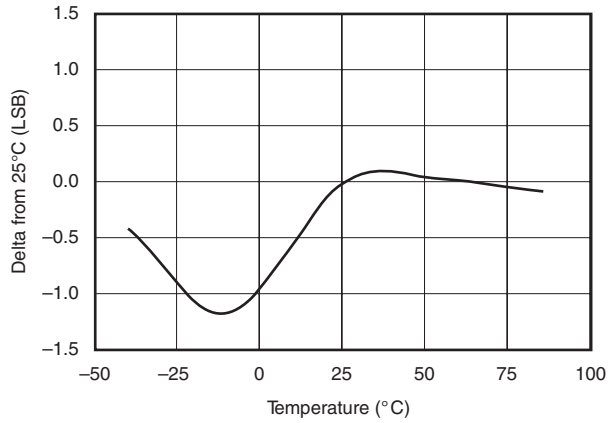


CHANGE IN OFFSET vs TEMPERATURE

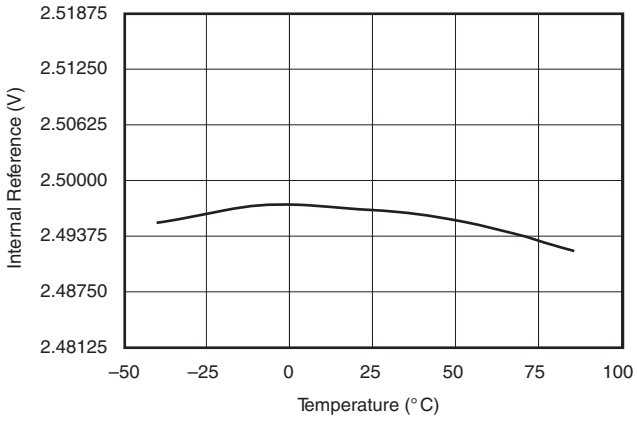


TYPICAL CHARACTERISTICS (continued)

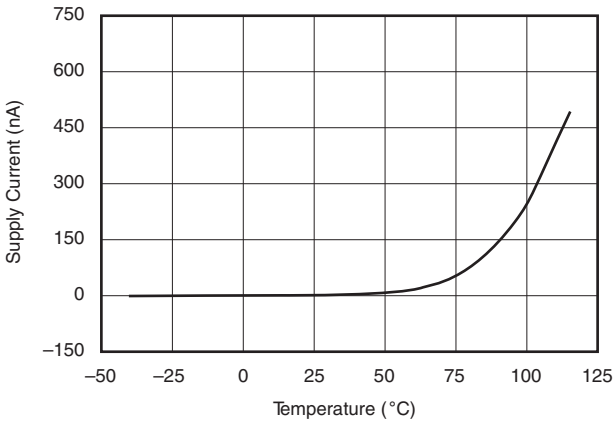
CHANGE IN GAIN vs TEMPERATURE



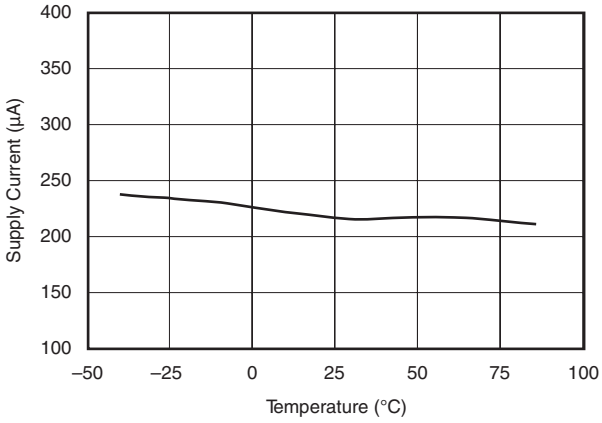
INTERNAL REFERENCE vs TEMPERATURE



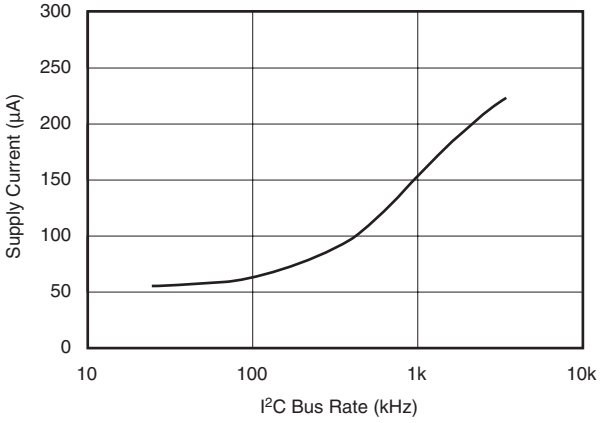
POWER-DOWN SUPPLY CURRENT vs TEMPERATURE



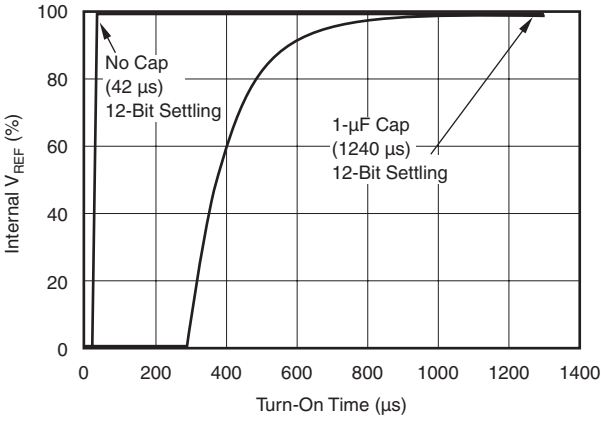
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs I²C BUS RATE



INTERNAL V_{REF} vs TURN-ON TIME



DEVICE INFORMATION

The ADS7828 is a classic Successive Approximation Register (SAR) A/D converter. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µ CMOS process.

The ADS7828 core is controlled by an internally generated free-running clock. When the ADS7828 is not performing conversions or being addressed, it keeps the A/D converter core powered off, and the internal clock does not operate.

The simplified diagram of input and output for the ADS7828 is shown in Figure 2.

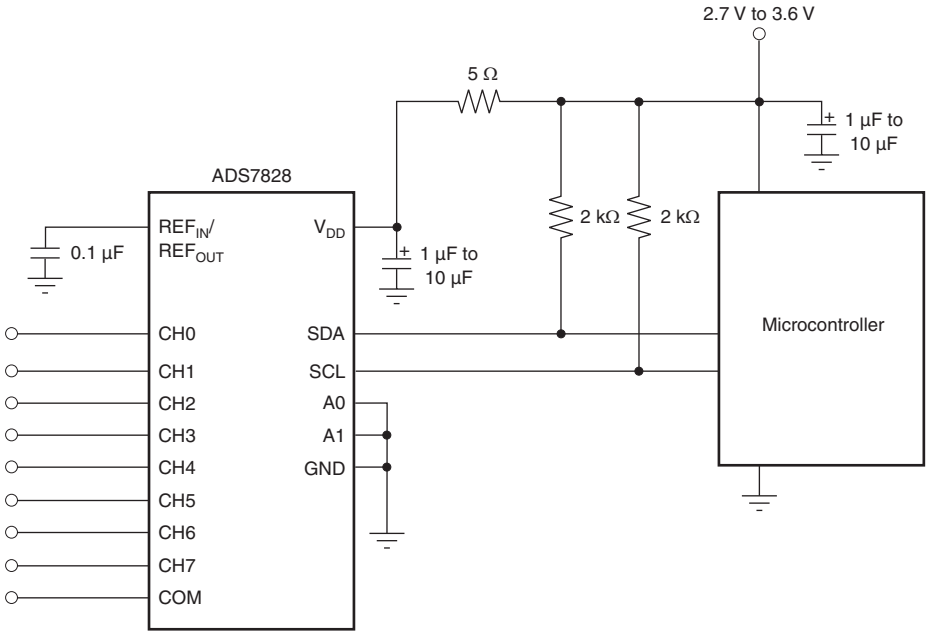


Figure 2. Simplified I/O Diagram

Analog Input

When the converter enters the hold mode, the voltage on the selected CHx pin is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25 pF). After the capacitor has been fully charged, there is no further input current. The amount of charge transfer from the analog source to the converter is a function of conversion rate.

Reference

The ADS7828 can operate with an internal 2.5-V reference or an external reference. If a 5-V supply is used, an external 5-V reference is required in order to provide full dynamic range for a 0 V to $+V_{DD}$ analog input. This external reference can be as low as 50 mV. When using a 2.7-V supply, the internal 2.5-V reference will provide full dynamic range for a 0 V to $+V_{DD}$ analog input.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 2.5-V reference, the internal noise of the converter typically contributes only 0.32 LSB peak-to-peak of potential error to the output code. When the external reference is 50 mV, the potential error contribution from the internal noise is 50 times larger—16 LSBs. The errors due to the internal noise are Gaussian in nature and can be reduced by averaging consecutive conversion results.

Digital Interface

The ADS7828 supports the I^2C serial bus and data transmission protocol, in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the Start and Stop conditions. The ADS7828 operates as a slave on the I^2C bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see Figure 3):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

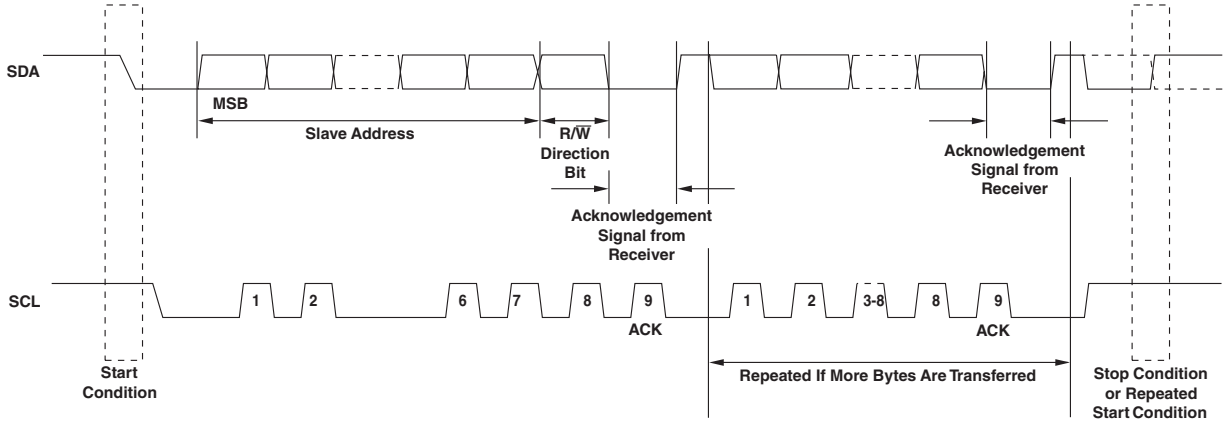


Figure 3. Basic Operation

Accordingly, the following bus conditions have been defined:

- Bus Not Busy

  Both data and clock lines remain high.
- Start Data Transfer

  A change in the state of the data line, from high to low, while the clock is high, defines a Start condition.
- Stop Data Transfer

  A change in the state of the data line, from low to high, while the clock line is high, defines the Stop condition.
- Data Valid

  The state of the data line represents valid data, when, after a Start condition, the data line is stable for the duration of the high period of the clock signal. There is one clock pulse per bit of data.

  Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.

  Within the I^2C bus specifications a standard mode (100-kHz clock rate), a fast mode (400-kHz clock rate), and a highspeed mode (3.4-MHz clock rate) are defined. The ADS7828 works in all three modes.
- Acknowledge

  Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

  A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition.

Figure 3 shows how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

- Data transfer from a master transmitter to a slave receiver.

  The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- Data transfer from a slave transmitter to a master receiver.

  The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned.

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or a repeated Start condition. Since a repeated Start condition is also the beginning of the next serial transfer, the bus will not be released.

The ADS7828 may operate in the following two modes:

- Slave Receiver Mode

  Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. Start and Stop conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- Slave Transmitter Mode

  The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the ADS7828 while the serial clock is input on SCL. Start and Stop conditions are recognized as the beginning and end of a serial transfer.

Address Byte

The address byte is the first byte received following the Start condition from the master device (see Figure 4). The first five bits (MSBs) of the slave address are factory pre-set to 10010. The next two bits of the address byte are the device select bits, A1 and A0. Input pins (A1-A0) on the ADS7828 determine these two bits of the device address for a particular ADS7828. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time.

MSB	6	5	4	3	2	1	LSB
1	0	0	1	0	A1	A0	R/$\overline{W}$

Figure 4. Address Byte

The A1/A0 address inputs can be connected to V_{DD} or digital ground. The device address is set by the state of these pins upon power-up.

The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. When set to a 1, a read operation is selected; when set to a 0, a write operation is selected. Following the Start condition, the ADS7828 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the 10010 code, the appropriate device select bits, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

The operating mode is determined by a command byte (see Figure 5).

MSB	6	5	4	3	2	1	LSB
SD	C2	C1	C0	PD1	PD0	X	X

Figure 5. Command Byte

SD: Single-ended or differential inputs

0 = Differential inputs

1 = Single-ended inputs

C2 to C0: Channel selections (see Table 1)

PD1, PD0: Power-down selection (see Table 2)

X: Unused

Table 1. Channel Selection Control Addressed by Command Byte

COMMAND BYTE INPUTS				CHANNEL SELECTIONS								
SD	C2	C1	C0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	0	+IN	–IN	—	—	—	—	—	—	—
0	0	0	1	—	—	+IN	–IN	—	—	—	—	—
0	0	1	0	—	—	—	—	+IN	–IN	—	—	—
0	0	1	1	—	—	—	—	—	—	+IN	–IN	—
0	1	0	0	–IN	+IN	—	—	—	—	—	—	—
0	1	0	1	—	—	–IN	+IN	—	—	—	—	—
0	1	1	0	—	—	—	—	–IN	+IN	—	—	—
0	1	1	1	—	—	—	—	—	—	–IN	+IN	—
1	0	0	0	+IN	—	—	—	—	—	—	—	–IN
1	0	0	1	—	—	+IN	—	—	—	—	—	–IN
1	0	1	0	—	—	—	—	+IN	—	—	—	–IN
1	0	1	1	—	—	—	—	—	—	+IN	—	–IN
1	1	0	0	—	+IN	—	—	—	—	—	—	–IN
1	1	0	1	—	—	—	+IN	—	—	—	—	–IN
1	1	1	0	—	—	—	—	—	+IN	—	—	–IN
1	1	1	1	—	—	—	—	—	—	—	+IN	–IN

Table 2. Power-Down Selection

PD1	PD0	DESCRIPTION
0	0	Power down between A/D converter conversions
0	1	Internal reference off and A/D converter on
1	0	Internal reference on and A/D converter off
1	1	Internal reference on and A/D converter on

Initiating Conversion

Provided the master has write-addressed it, the ADS7828 turns on the A/D converter section and begins conversions when it receives bit 4 of the command byte shown in Figure 5. If the command byte is correct, the ADS7828 returns an ACK condition.

Reading Data

Data can be read from the ADS7828 by read addressing the part (LSB of address byte set to 1) and receiving the transmitted bytes. Converted data can be read from the ADS7828 only after a conversion has been initiated as described in the preceding section.

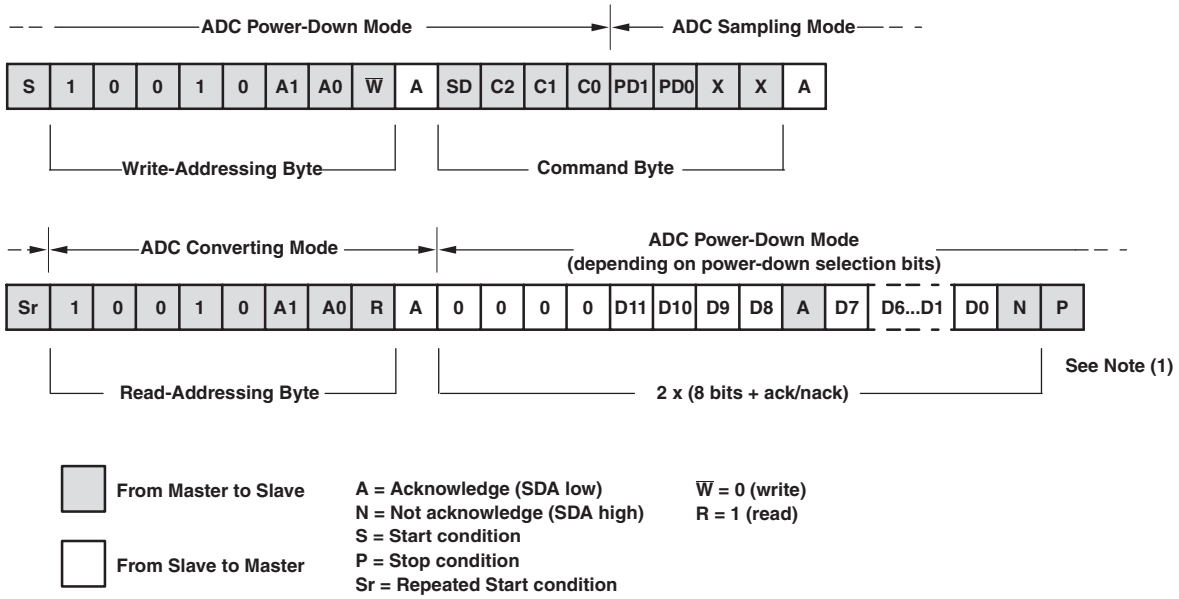
Each 12-bit data word is returned in two bytes (see Figure 6), where D11 is the MSB of the data word, and D0 is the LSB. Byte 0 is sent first, followed by byte 1.

	MSB	6	5	4	3	2	1	LSB
Byte 0	0	0	0	0	D11	D10	D9	D8
Byte 1	D7	D6	D5	D4	D3	D2	D1	D0

Figure 6. Reading Data

Reading in Fast or Standard (F/S) Mode

Figure 7 shows the interaction between the master and the slave ADS7828 in fast or standard (F/S) mode. At the end of reading conversion data, the ADS7828 can be issued a repeated Start condition by the master to secure bus operation for subsequent conversions of the A/D converter. This would be the most efficient way to perform continuous conversions.



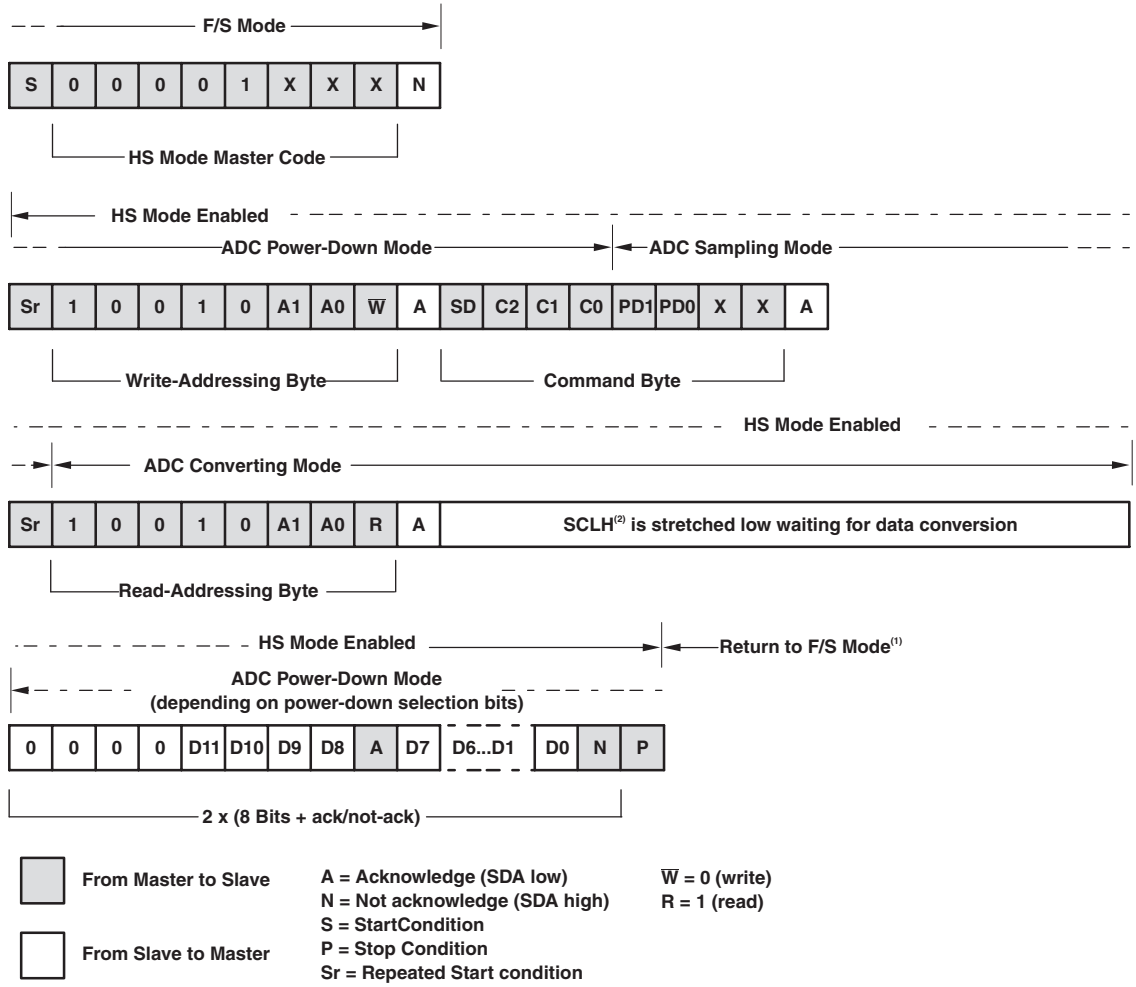
NOTE: (1) To secure bus operation and loop back to the stage of write-addressing for next conversion, use Repeated Start.

Figure 7. Typical Read Sequence in F/S Mode

Reading in High-Speed (HS) Mode

High Speed (HS) mode is fast enough that codes can be read out one at a time. In HS mode, there is not enough time for a single conversion to complete between the reception of a repeated Start condition and the read-addressing byte, so the ADS7828 stretches the clock after the read-addressing byte has been fully received, holding it low until the conversion is complete.

See Figure 8 for a typical read sequence for HS mode. Included in the read sequence is the shift from F/S to HS modes. It may be desirable to remain in HS mode after reading a conversion; to do this, issue a repeated Start instead of a Stop at the end of the read sequence, since a Stop causes the part to return to F/S mode.



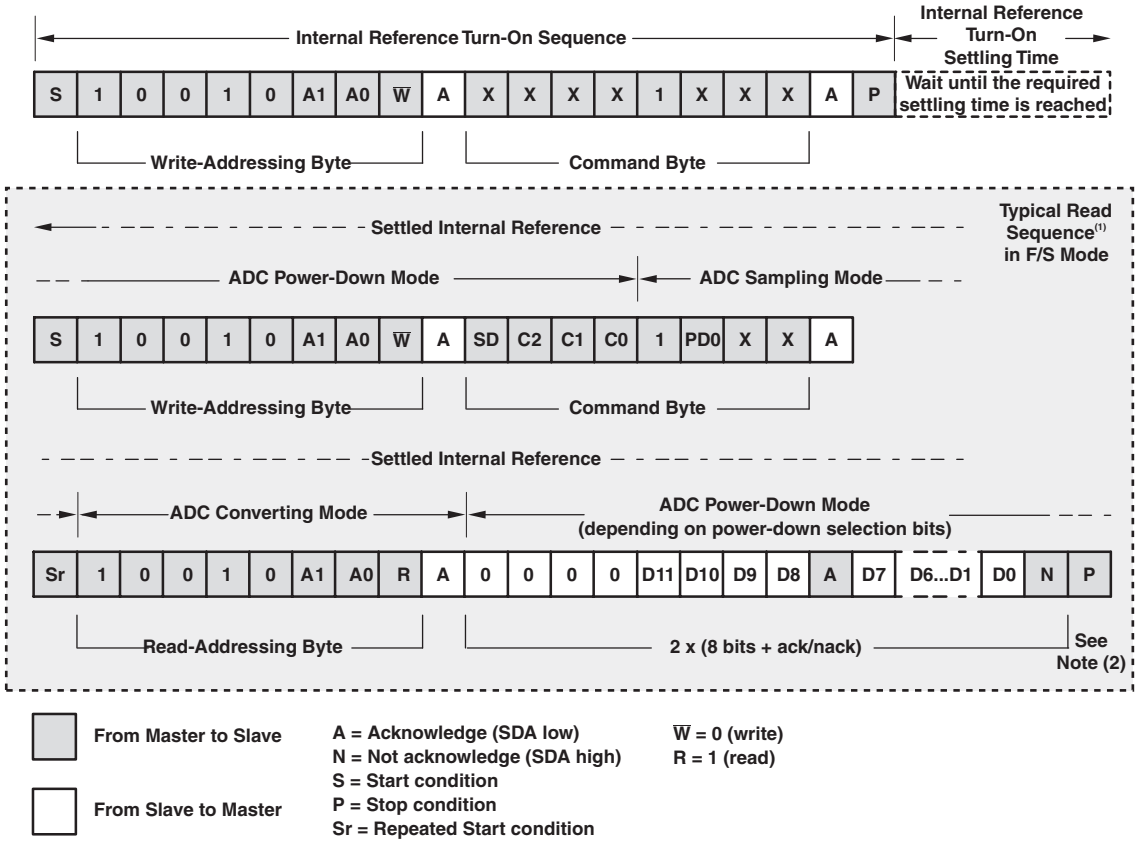
NOTES: (1) To remain in HS mode, use Repeated Start instead of Stop.
(2) SCLH is SCL in HS mode.

Figure 8. Typical Read Sequence in HS Mode

Reading With Reference On/Off

The internal reference defaults to off when the ADS7828 power is on. To turn the internal reference on or off, see Table 2. If the reference (internal or external) is constantly turned on and off, a proper amount of settling time must be added before a normal conversion cycle can be started. The exact amount of settling time needed varies depending on the configuration.

See Figure 9 for an example of the proper internal reference turn-on sequence before issuing the typical read sequences required for the F/S mode when an internal reference is used.



NOTES: (1) Typical read sequences can be reused after the internal reference is settled.
(2) To secure bus operation and loop back to the stage of write-addressing for next conversion, use Repeated Start.

Figure 9. Internal Reference Turn-On Sequence and Typical Read Sequence (F/S Mode Shown)

When using an internal reference, there are three things that must be done:

1. To use the internal reference, the PD1 bit of Command Byte must always be set to logic 1 for each sample conversion that is issued by the sequence, as shown in Figure 7.
2. To achieve 12-bit accuracy conversion when using the internal reference, the internal reference settling time must be considered, as shown in the Internal VREF vs Turn-On Time Typical Characteristic plot. If the PD1 bit has been set to logic 0 while using the ADS7828, then the settling time must be reconsidered after PD1 is set to logic 1. In other words, whenever the internal reference is turned on after it has been turned off, the settling time must be long enough to get 12-bit accuracy conversion.
3. When the internal reference is off, it is not turned on until both the first Command Byte with PD1 = 1 is sent and then a Stop condition or repeated Start condition is issued. (The actual turn-on time occurs once the Stop or repeated Start condition is issued.) Any Command Byte with PD1 = 1 issued after the internal reference is turned on serves only to keep the internal reference on. Otherwise, the internal reference would be turned off by any Command Byte with PD1 = 0.

The example in Figure 9 can be generalized for an HS mode conversion cycle by changing the timing of the conversion cycle. If using an external reference, PD1 must be set to 0, and the external reference must be settled. The typical sequence in Figure 7 or Figure 8 can then be used.

PCB Layout

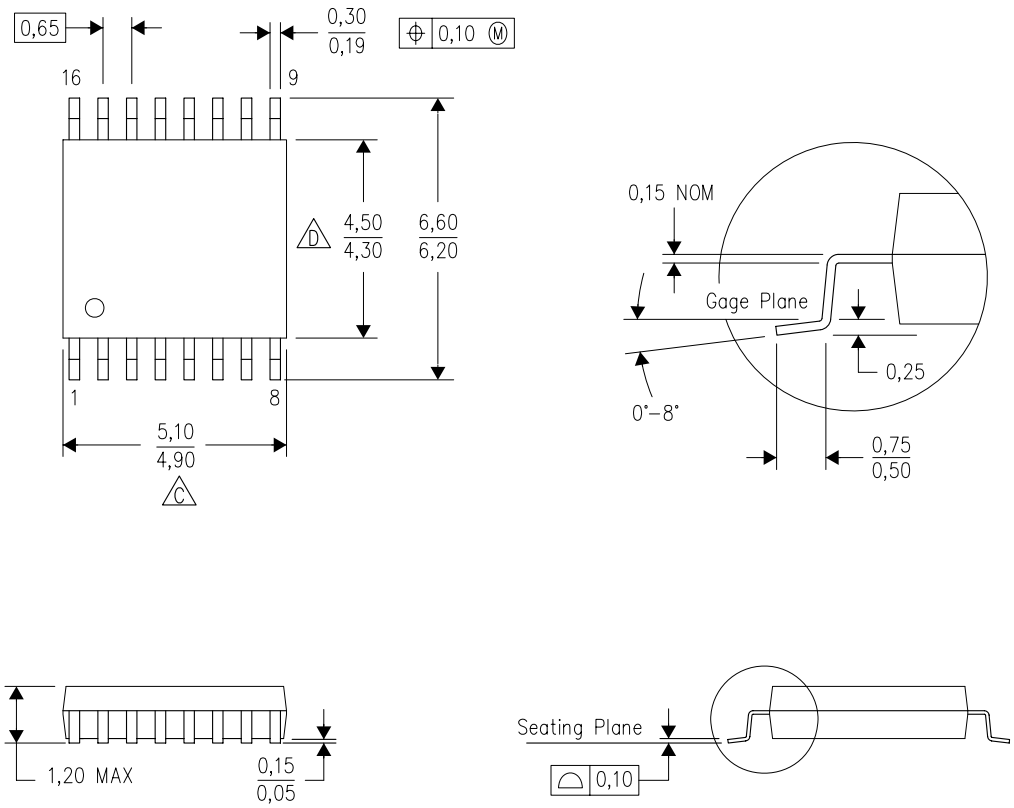
For optimum performance, care should be taken with the physical layout of the ADS7828 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an "n-bit" SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices.

With this in mind, power to the ADS7828 should be clean and well-bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. A 1-µF to 10-µF capacitor may also be needed if the impedance of the connection between $+V_{DD}$ and the power supply is high.

The ADS7828 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50 Hz or 60 Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

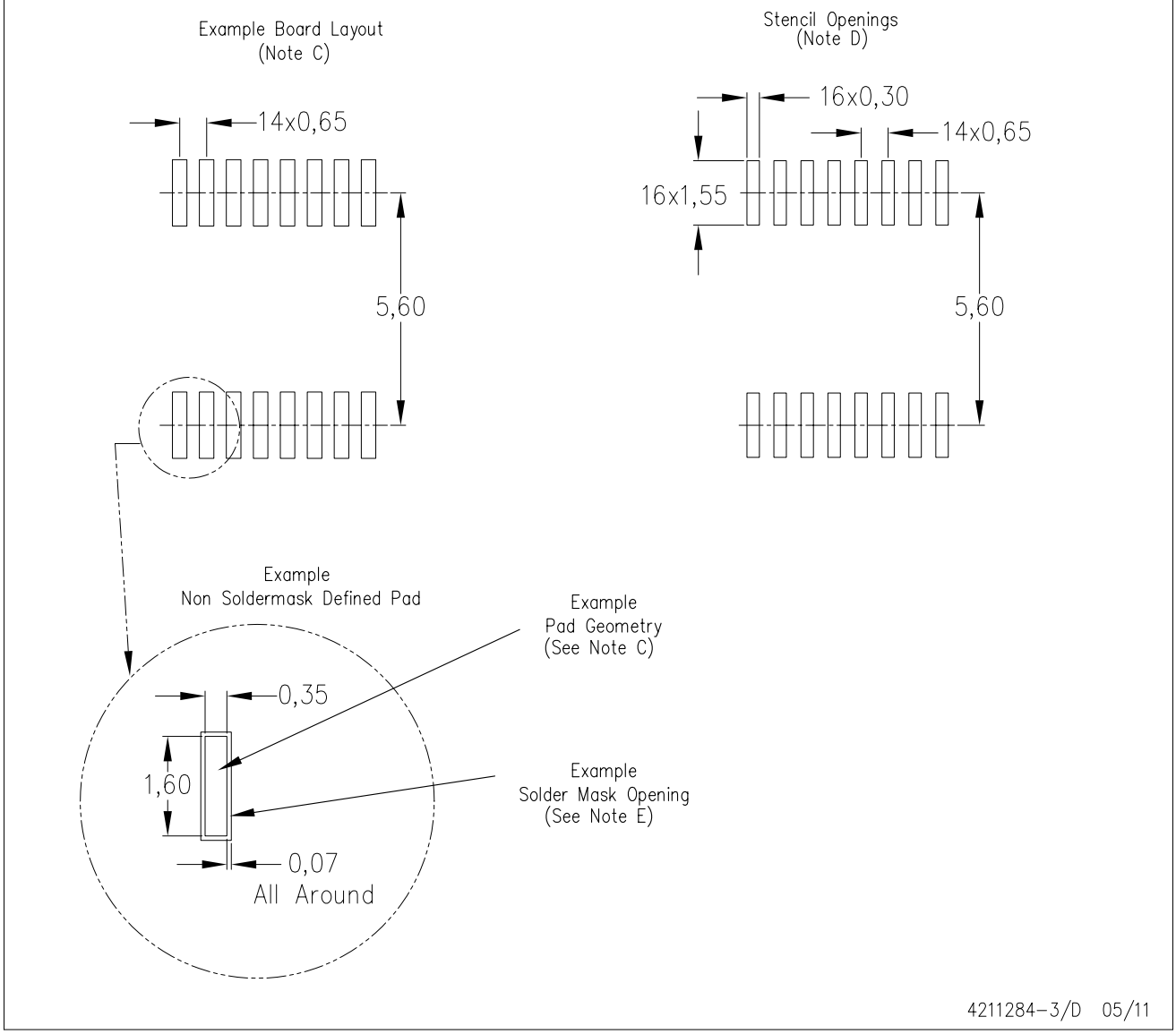
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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